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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,448	04/02/2004	Matti Floman	944-003.225	1610
4955	7590	12/08/2006	EXAMINER	
WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP BRADFORD GREEN, BUILDING 5 755 MAIN STREET, P O BOX 224 MONROE, CT 06468			DOAN, DUC T	
			ART UNIT	PAPER NUMBER
			2188	

DATE MAILED: 12/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/817,448

Applicant(s)

FLOMAN ET AL.

Examiner

Duc T. Doan

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22, 33 and 34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22, 33 and 34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Status of Claims

Claims 1-22 have been presented for examination in this application. In response to the last office action, claims 1-22 have been elected without traverse for prosecution, claims 23-32 have been canceled, claims 33-34 have been added, claims 1-3,6-8,11-13,15-18,20 have been amended. As the result, claims 1-22,33-34 are pending in this application.

Claims 1-22,33-34 are rejected.

U.S.C. 112, first paragraph

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 33-34 are rejected under 35 U.S.C. 112, first paragraph,

As in claim ~~33~~¹³, the claim is rejected since it discloses a single mean claim, wherein a means recitation does not appear in combination with another recited element of means (see MPEP 2164.08(a)).

All dependent claim(s) are rejected as having the same deficiencies as the base claims that they depend from.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1,3-4,8,20-22,33 are rejected under 35 U.S.C. 102 (e) as being anticipated by Ganton (US 6792499).

As in claim 1, Ganton discloses a memory module comprising: a fast nonvolatile random access memory, responsive to a command/data signal provided by a processor (Ganton's Fig 1 discloses a fast non-volatile random access memory #115 responsive to processor CPU using a command address data signals, see Ganton's paragraph 11), for providing a permanent storage of information before said command/data signal is provided, for executing a command comprised in said command/data signal using said permanently stored information (Ganton's paragraph 25 non-volatile memory provides storages for operating systems, program code, applications, radio

calibration parameters and phone books information, Ganton's paragraph 30 further discloses executing using code permanently stored in the non-volatile random access memory), for providing a direct communication between said non-volatile random access memory and the processor (Ganton's Fig 1, command address/data signal providing direct communication between non-volatile memory and processor).

As in claims 3-4, wherein the fast non-volatile random access memory provides a temporal storage of data (claim 3, Ganton's paragraph 28 discloses non-volatile random access memory stores temporary data such as recent call lists); wherein said fast non-volatile random access memory comprises an information storage area for permanent storage of said information; and a temporal data storage area for the temporal storage of said data (claim 4, Ganton's paragraph 28 discloses the non-volatile storage stores permanently information such as operating system and temporary data such as phone book, recent call lists).

As in claim 8, Ganton discloses wherein said information comprises an application program for operating an electronic device (Ganton's paragraph 25 discloses information comprises program codes, applications, radio calibration parameters and phonebook information).

Claim 20 rejected based on the same rationale as of claim 1.

As in claims 21-22, Ganton discloses a power and reset block, for resetting said processor and for resetting said fast non-volatile random access memory; wherein said electronic device is a portable electronic device, a mobile electronic device or a mobile phone (claim 21, power supplying and resetting circuitry for a system is represented in Ganton's Fig 7: #26, paragraph 4 the device is a mobile phone etc..).

Claim 33 rejected based on the same rationale as of claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499) as applied to claim 1, and in view of Lin (US 7032105).

As in claim 2, Ganton discloses the memory controller includes well known in the art convert circuitry to converting different protocol for interfaces with different memory devices such as non-volatile, sram, sdram etc.. Ganton further discloses using different clock edges to convert and clocking data in different memory interfaces. Ganton does not expressly disclose the double rate DDR type interface. However, Lin discloses a memory controller having SDRAM and DDR interface conversion circuitry (Lins's column 4 lines 35-39, Fig 1: #74). It would have been obvious to one of ordinary skill in the art at the time of invention to include conversion circuit and the memory storing method as suggested by Lin in Ganton's system to convert load/store commands issued by the CPU into appropriate memory access commands for

accessing DDR dynamic random memory, thereby providing the system with a fast efficient method to store data into DDR DRAM in a permanent manner, see Lin's column 3 lines 57-67).

Claims 5-7 rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499) as applied to claim 1, and in view of Witek et al (US 7093153).

As in claim 5, Ganton does not expressly disclose at least one register for setting operating parameters of the fast non-volatile random access memory or protecting said data or said information during said execution. However, Witek discloses a controller having set of registers for setting operating parameters of the memory devices such as sdram, sram, and non-volatile memory devices (Witek's column 5 lines 40-65). It would have been obvious to one of ordinary skill in the art at the time of invention to include registers sets in memory controllers as suggested by Witek in Ganton's system to allow hardware logic to optimize the memory devices operation dynamically in an efficiently manner, thereby to further reduce the power consumption of the overall system (Witek's column 2 lines 1-10).

As in claim 6, Witek further discloses wherein said operating parameters comprises one or more of a timings for a particular frequency, and frequency ranges with a corresponding core voltage range (Witek's Fig 1 discloses a phase lock loop logic provides timing for a particular frequency, and providing clocks in a range of frequencies. Witek's column 6 lines 8-50 further discloses the operating parameters are used to optimizing the devices' operating frequencies corresponding to the core voltages being used in the devices, thus the overall power consumption of the system can be reduced).

As in claim 7, Witek's column 5 lines 55-64 further discloses the set of register (i.e address region control registers) are used to protect write to a region, for example write to a read only region will be protected.

Claims 9-11,13-18,34 rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499) as applied to claim 1, and in view of Pua et al (US 2005/0041473).

As in claim 9, Ganton does not expressly disclose a mass memory, for providing further information in response to a command/information signal, However, Pua's Fig 2 discloses a memory controller (Pua's Fig 2: #12 controlling IC) comprises a mass memory (memory attaching to the Fig 2: #131 NAND IC terminal) that provides more storages to store information in response to a command/information signal request from the controlling IC (see Pua's paragraph 20 lines 13-16). It would have been obvious to one of ordinary skill in the art at the time of invention to include memory controller capable of controlling multiples memory devices as suggested by Pua in Ganton's system, thereby extra memory capacity can be readily added in the system (Pua's paragraph 20 lines 13-16). Ganton further discloses that an application-specific integrate circuit is employed to provide command/information signal to memory device (Ganton's Fig 5, paragraph 33).

As in claim 10, Pua's Fig 2 discloses wherein said further information is provided to say fast non-volatile random access memory (information of memory attaching to Pua's Fig 2: #131 is provided to non-volatile memory Fig 2: #13).

As in claim 11, Pua discloses information in the extend memory attached to Pua's Fig 2: #131, is provided to the non-volatile random access memory (Pua's Fig 2: #13), this information will be used/processed by the processing element (Ganton's Fig 5: #525, paragraph 34).

As in claim 13, Ganton discloses a non-volatile random access memory integrate circuit package comprises the application specific integration circuit (Ganton's Fig 1: #105, serial memory interface controller), the mass memory and the fast non-volatile random access memory (Ganton's Fig 1: #115), Pua further disclose a mass memory readily attached to the system to increase the total capacity of the memory system (memory attached to Pua's Fig 2: #131) or the application specific integration circuit (Ganton's Fig 1: #105, serial memory interface controller), and the fast non-volatile random access memory (Ganton's Fig 1: #115), or the mass memory and the non-volatile random access memory (Ganton Fig 3, paragraph 31, discloses another embodiment in which the processor having extra circuitry to provide reading/processing boot code in the onboard ROM Fig 1: #307, thus the circuitry in the memory interface (Fig 3: #310) is reduced to merely carrying out the command/data from the processor (Fig 3: CPU)).

As in claim 14, Pua discloses the memory controller (Pua's #12) comprises multiples memory interfaces (Fig 1: #15 I/O interface, #16 memory card interface, #17 memory interface, and memory IC #14) for provide additional mass memories to the system. Pua does not expressly disclose additional memory as a dynamic random access memory, however, using the dynamic random access memory has been known in the art (see Ganton's paragraph 28 lines 8-11).

Claim 15 rejected based on the same rationale as in claim 13 and 14.

As in claim 16, Ganton discloses the dynamic random access memory is loaded with code (images is stored in SDRAM); this code is readily for used by the CPU.

As in claim 17, Pua discloses removable mass memory (memory attaching to Fig 2: #131 nand ic terminal, #1411 sram ic terminal) provided further information to the fast non-volatile random access memory (Pua's Fig 2: #13) or to sram IC #141 or to both #13 and #141 in response to a further command/information signal provides by the application specific integration circuit (Pua's Fig 2: #12 control IC). Although Pua does not expressly disclose the extend memory sram IC #141 can be a dynamic random access memory. However, a dynamic random access memory can readily be used to extend memory capacity in the system as disclosed by Ganton's paragraph 28 lines 8-11.

As in claim 18, the claim rejected based on the same rationale of claims 14 and 17.

As in claim 34, Pua further discloses the circuitry is integrated into a module (Pua's paragraph 7).

Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499), Pua et al (US 2005/0041473) as applied to claim 9, and in view of Lin (US 7032105).

Claim 12 rejected based on the same rationale as of claim 2.

Claim 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US 6792499) as applied to claim 1, and in view of Coufal et al (IBM Technical Disclosure Bulletin, Vol 37 No. 11 November 1994, pp 421-424).

As in claim 19, Ganton and Pua do not expressly disclose the fast non-volatile random access memory is a magneto-resistive random access memory, a ferroelectric random access

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memory, or an Ovonic memory type. However, Coufal discloses a non-volatile random access memory is build as a ferroelectric random access memory (Coufal's first paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to include a ferroelectric random access memory by Coufal in Ganton's system thereby further providing a fast non-volatile random access memory with a huge memory capacity (Coufal's first paragraph, fast access time, and high memory density, third paragraph).

Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

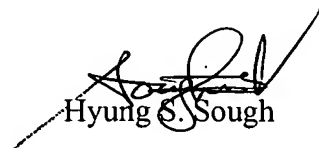
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Duc Doan

Examiner

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Hyung S. Sough

12/07/06

Supervisory Patent Examiner

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